REMARKS

Claims 6-7, 17-18 and 25-27 were objected to as being dependent on a rejected base claim. Applicant thanks the Examiner for the indication of allowable subject matter.

Claims 1-3, 8-10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lomp in view of Adelmann. Applicant respectfully traverses the rejection and requests reconsideration.

In claim 1, Applicant claims "a memory storing both programming instructions and ADPCM encoded source file data." The Examiner points to a discussion of Figure 19 of Adelmann at col. 24, lines 43-58. Applicant first notes that although Adelmann mentions a read only memory (ROM), there is no teaching in Adelmann for the specifically claimed memory. The reason for this is because Applicant claims more than just a memory. The claim language specifically requires that the memory store both programming instructions and ADPCM encoded source file data. While Adelmann includes a ROM, there is no teaching or suggestion in Adelmann for that memory storing the claimed programming instructions and ADPCM encoded source file data. To meet this limitation, the Examiner apparently points to Adelmann col. 24, lines 50-55 where there is made mention of ADPCM. This simple mentioning of ADPCM does not rise to the level of a teaching for a memory that stores both programming instructions and ADPCM encoded source file data. In fact, a careful reading of the text cited by the Examiner reveals that the teaching in Adelmann is for a BDI field which contains information which can be used to address the ROM. From addressing the ROM, one can obtain a receive status signal and packet length signal (col. 24, lines 45-47). The receive status signal "indicates the type of coding" such as ADPCM which was employed by the transmitter. Thus, the ROM in Adelmann DOES NOT store BOTH programming instructions and ADPCM encoded source file data, but rather stores a simple indicator of what type of coding was used for a given communication. This teaching is not relevant to the specific claim limitations and language at issue. The cited portion of Adelmann relied upon by the Examiner wholly fails to teach or suggest the claimed

"memory storing both programming instructions and ADPCM encoded source file data." The prima facie case for a Section 103 rejection accordingly has not been met.

To the extent the Examiner asserts that the Adelmann ROM, which notably is "not shown" in Figure 19 (col. 24, lines 44-45), meets the claimed "memory storing both programming instructions and ADPCM encoded source file data," Applicant respectfully requests that the Examiner specifically point out where in Adelmann such a teaching is presented.

In claim 1, Applicant further claims "a micro-controller having an architecture that implements time multiplexed memory addressing." The Examiner points to Adelmann Figure 25 as meeting this limitation. Applicant respectfully disagrees and asks the Examiner to particularly point out where in Adelmann Figure 25 there is a micro-controller which implements time multiplexed memory addressing. There is no memory shown in Figure 25. As discussed above, the Examiner notes a teaching in Adelmann for ROM, but there is no teaching that this ROM stores the "programming instructions and ADPCM encoded source file data" which is claimed. Still further, there is no teaching in Adelmann Figure 25 for performance of a time multiplexed memory addressing operation. In fact, the Examiner's analysis in the office action wholly fails to identify what specific portion of Adelmann Figure 25 is asserted to perform time multiplexed memory addressing. Applicant respectfully submits that there is no teaching in Adelmann for the claimed operation and requests that the Examiner specifically point out what aspects of Adelmann are being relied upon to meet the "micro-controller having an architecture that implements time multiplexed memory addressing" limitation of claim 1. The prima facie case for a Section 103 rejection has not been met.

Still further, Applicant claims in claim 1 first and second cycles of operation. The Examiner points to Adelmann Figure 25 as meeting this limitation. Applicant respectfully disagrees and asks the Examiner to particularly point out where in Adelmann Figure 25 there is a teaching for the cycled memory access operations which are claimed. In the cited portion of Adelmann there is a teaching for the processing of samples. However, this sample processing

hardly meets the recited limitations relating in general to first and second cycles, and in particular to memory access cycles for extracting ADPCM encoded source file data in a first cycle and extracting programming instructions in a second cycle. The prima facie case for a Section 103 rejection has not been met. Applicant further requests that the Examiner specifically point out what aspects of Adelmann are being relied upon to meet the first and second cycle operation limitations of claim 1.

Lastly, Applicant points out that in addressing the "a micro-controller having an architecture ..." limitation of claim 1, the Examiner generally points to Figure 25 and specification columns 30 and 31 of Adelmann. However, the Examiner fails to particularly point out what portions of columns 30-31, or Figure 25, are being relied upon to meet each specifically recited limitation of the claim. The Examiner is accordingly reminded of the requirements of 37 CFR 1.104(c)(2) concerning designating for the Applicant in the Office Action the particular part(s) of a reference being relied upon, as well as explaining the pertinence of the reference to the claimed invention. In the present case, Applicant respectfully submits that the Examiner's unfocused citation to two columns of the Adelmann reference without any indication as to how the features of the Adelmann disclosure apply to the claimed "micro-controller," "time multiplexed memory addressing," "first cycle" delivery of "ADPCM encoded source file data," and "second cycle" delivery of "programming instructions," limitations not only fails to satisfy the Examiner's burden under Rule 1.104(c)(2) but further fails to satisfy the Examiner's burden under 35 U.S.C. 103(a) to make out the prima facie case for obviousness. Reconsideration of the rejection is requested. Furthermore, to the extent the Examiner chooses to maintain the rejection, Applicant requests that the Examiner precisely identify how the cited prior art references are being used to meet each and every limitation of the claims.

Claims 2-3 and 8-10 depend from claim 1 and are asserted to be patentable over the cited prior art for at least the same reasons as claim 1. Applicant additionally points out, with respect to claim 8, that as there is no teaching in Adelmann for the claimed first and second cycles, there can be no teaching for the claim 8 recitation to repeat the first and second cycles. The Examiner

cites to Adelmann col. 7 lines 35-47 as meeting this limitation. Applicant disagrees. The cited teaching of Adelmann concerns ADPCM output generation. The claim language refers to both the first and second cycles, and thus implicates alternating ADPCM processing (first cycle) and programming instruction processing (second cycle). The Examiner has failed to show how the cited portion of Adelmann teaches or suggests the repeating and alternating first and second cycle operations as claimed. Withdrawal of the Section 103 is requested. Additionally, Applicant requests that the Examiner more particularly identify how Adelmann meets both of the first and second cycle operations as recited in claims 1 and 8.

Claims 4, 15, 19-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lomp and Adelmann in view of Childers and Zeilenga.

Applicant respectfully traverses and asserts that claim 4 is patentable over the cited prior art for at least the reasons recited above with respect to claim 1. Additionally, Applicant notes that the Examiner has picked a program counter and address counter from Childers and a multiplexer from Zeilenga to meet the limitations of claim 4. The Examiner is well aware of the requirement for there to be a teaching for combining references. In connection with the discussion of claim 4, the Examiner has failed to indicate why one of skill in the art would combine the teachings of Childers and Zeilenga together to make a micro-controller as claimed. Additionally, the Examiner has failed to indicate why one of skill in the art would combine the Childers/Zeilenga circuit into the Adelmann design. What is the motivation to combine this art? Applicant respectfully submits that there is no motivation to combine. Additionally, even if such a motivation existed, the resulting combination would still not meet the claimed invention as there is no teaching in any of the references for having the memory store both programming instructions and ADPCM encoded source file data. Withdrawal of the Section 103 rejection of claim 4 is requested.

With respect to claim 15, while Zeilenga teaches a multiplexer, there is no teaching or suggestion in any of the references, taken alone or in combination, for multiplexer selected "first and second memory addresses" to relate to a selection of "the first memory address for

application to the memory during a first cycle" and related to a selection of "the second memory address for application to the memory during a second cycle" where the first memory addresses relate to stored programming instructions and the second memory addresses related to stored adaptive differential pulse code modulation (ADPCM) encoded source file data. As discussed above, the Lomp and Adelmann references wholly fail to teach or suggest the claimed memory, the claimed information stored in the memory, or the claimed first and second cycles relating to the stored information. Withdrawal of the Section 103 rejection is requested.

Claims 19-20 depend from claim 15 and are asserted to be patentable over the cited prior art for at least the reasons recited with respect to claim 15.

Claims 5, 11-14, 16, 21-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lomp and Adelmann in view of Childers, Zeilenga and Lesmeister. Applicant respectfully traverses and asserts that claim 5 is patentable over the cited prior art for at least the reasons recited above with respect to claim 1. Additionally, claims 11-14, which were rejected by the Examiner as being method claims corresponding to claims 1-5, are asserted by Applicant to be patentable over the cited prior art for at least the reasons recited above with respect to claim 1. Claim 16 is asserted by Applicant to be patentable over the cited prior art for at least the reasons recited above with respect to claim 15.

Claims 21-24, which were rejected by the Examiner for the same reasons as claims 1-4, are asserted by Applicant to be patentable over the cited prior art for at least the reasons recited above with respect to claim 1.

In view of the foregoing, Applicants submit that the application is now in condition for favorable action and allowance.

Respectfully submitted,

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